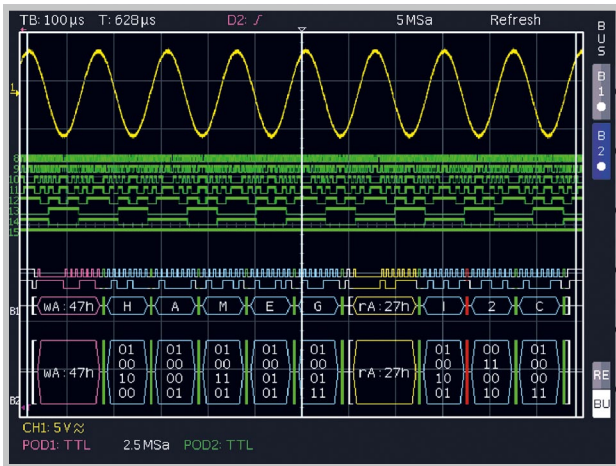
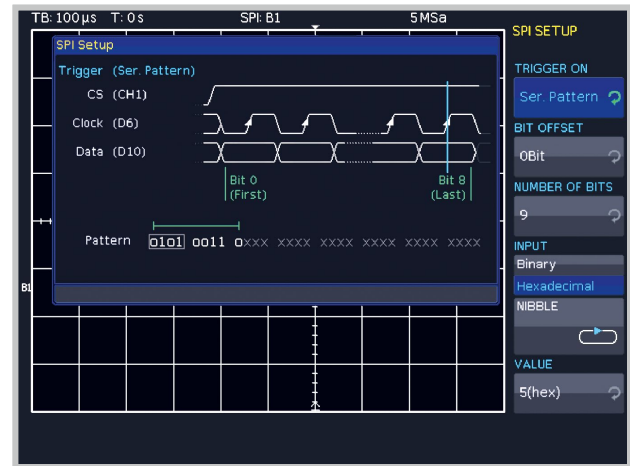


H0010/H0011 Serial Bus

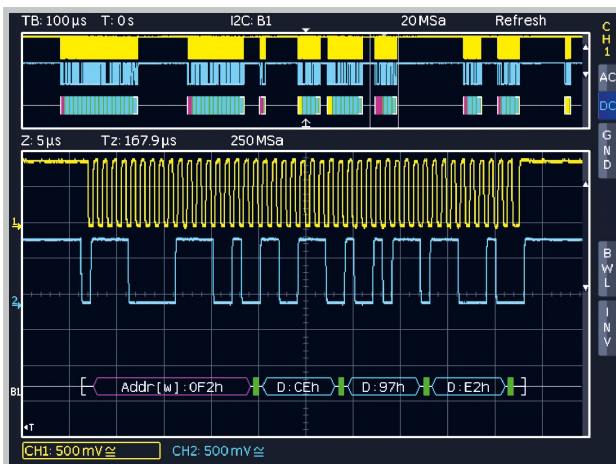
for all Oscilloscopes of the HMO Series



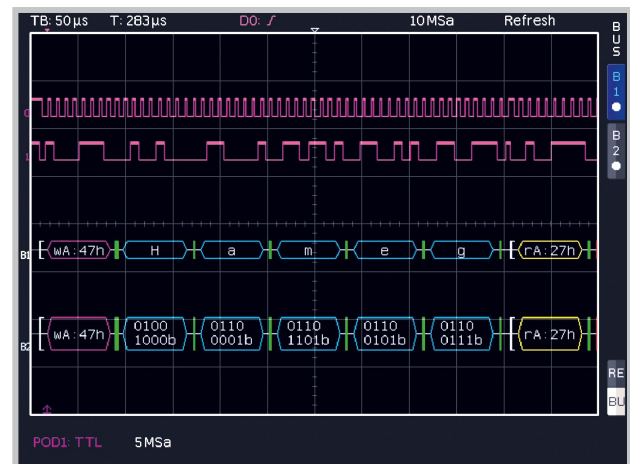
Mixed Signal and Bus Display



SPI Bus Trigger Setup



I²C Bus Hex decoding on the Analog Channel



I²C Bus ASCII and Binary

- ✓ H0010 via Analog Channels and/or Logic Channels, H0011 via Analog Channels
- ✓ I²C, SPI, UART/RS-232 Bus Trigger and Decode
- ✓ Hardware accelerated Decode in Real Time
- ✓ Color Coded Display of the Content for intuitive Analysis and easy Overview
- ✓ More Details of the decoded Values become visible with increasing Zoom Factor
- ✓ Bus Display with synchronous Display of the Data and, if selected, Clock Signal
- ✓ Decode into ASCII, Binary, Hexadecimal or Decimal Format
- ✓ Up to four Lines to comfortably show the decoded Values
- ✓ Powerful Trigger to isolate specific Messages
- ✓ Option for all Oscilloscopes of the HMO Series, retrofittable

H0010/H0011 I²C, SPI, UART/RS-232 Bus Analysis

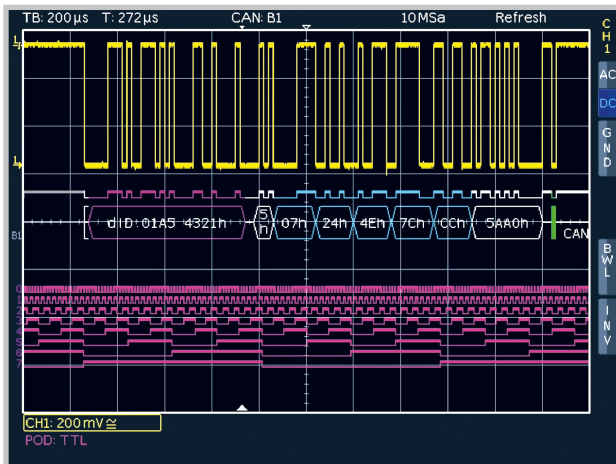
H0010/H0011 I ² C, SPI, UART/RS-232 Bus Analysis			
	I ² C Bus	SPI Bus	UART/RS-232 Bus
Bus Configuration			
Bit/Baud rate	up to 10 Mbit/s (HMO352x/2524), up to 5 Mbit/s (HMO72x...202x)	up to 25 Mbit/s (HMO352x/2524), up to 12.5 Mbit/s (HMO72x...202x)	300, 600, 1,200, 2,400, 4,800, 9,600, 19,200, 38,400, 57,600, 115,200 Baud, up to 62.5 Mbit/s (HMO352x/2524), up to 31 Mbit/s (HMO72x...202x)
Number of Bit's	7 or 10 Bit for Address ID 8 Bit for Data	32 Bit for Data	8 Bit for Data 1, 1.5, 2 Bit for Stop Bit
Polarity	n/a	Chip Select, positive or negative, or without Chip Select (2-wire SPI) Clock rising or falling edge Data High or Low active	High or Low active
Parity	n/a	n/a	none, odd or even
Trigger			
Source	H0010: digital Channels LCH 0...15 [Opt. H03508] analog Channels CH 1...2 [CH 1...4] H0011: analog Channels CH 1...2 [CH 1...4]	H0010: digital Channels LCH 0...15 [Opt. H03508] analog Channels CH 1...2, external Trigger Entry for Chip Select, [CH 1...4] H0011: analog Channels CH 1...2, external Trigger Entry for Chip Select, [CH 1...4]	H0010: digital Channels LCH 0...15 [Opt. H03508] analog Channels CH 1...2 [CH 1...4] H0011: analog Channels CH 1...2 [CH 1...4]
Event	7 or 10 Bit Address ID 7 or 10 Bit Address ID with 8 Bit Data Start, Stop, Restart missing Acknowledge Address ID without Acknowledge	Data packets up to 32 Bit with positive or negative Chip Select or without Chip Select, (2-wire SPI)	Data packets up to 8 Bit
Input format	Hexadecimal or Binary	Hexadecimal or Binary	Hexadecimal or Binary
Hardware accelerated Decode			
Source	H0010: digital Channels LCH 0...15 [Opt. H03508] analog Channels CH 1...2 [CH 1...4] H0011: analog Channels CH 1...2 [CH 1...4]	H0010: digital Channels LCH 0...15 [Opt. H03508] analog Channels CH 1...2, external Trigger Entry for Chip Select, [CH 1...4] H0011: analog Channels CH 1...2, external Trigger Entry for Chip Select, [CH 1...4]	H0010: digital Channels LCH 0...15 [Opt. H03508] analog Channels CH 1...2 [CH 1...4] H0011: analog Channels CH 1...2 [CH 1...4]
Display	Bus display, color coded for Read Address ID: Yellow Write Address ID: Magenta Data: Cyan Start: White Stop: White ACK/NACK: Green/Red Error: Red Trigger Condition: Green up to four lines for decoded values, synchronous display of the Bit lines	Bus display, color coded for Data: Cyan Start: White Stop: White Error: Red Trigger Condition: Green up to four lines for decoded values, synchronous display of the Bit lines	Bus display, color coded for Data: Cyan Start: White Stop: White Error: Red Trigger Condition: Green up to four lines for decoded values, synchronous display of the Bit lines
Format	Address ID: hexadecimal Data: ASCII, binary, decimal, hexadecimal	n/a Data: ASCII, binary, decimal, hexadecimal	n/a Data: ASCII, binary, decimal, hexadecimal

Differences H0010/H0011

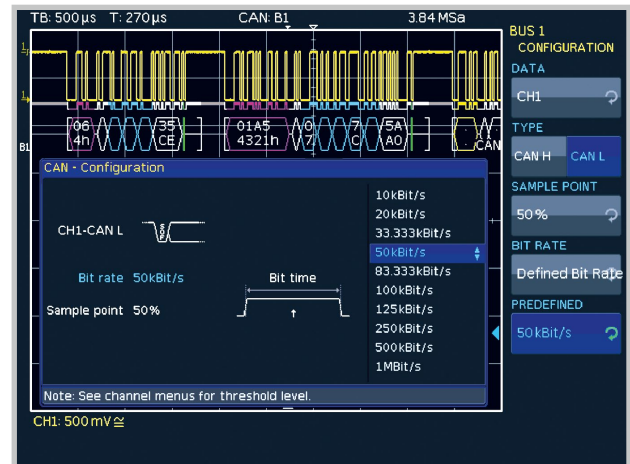
Feature	H0010	H0011
Logic Channels (LCH 0...LCH 15) as source for serial bus trigger and decode	x	-
Analog Channels (CH 1...CH 4) as source for serial bus trigger and decode	x	x
Time synchronous decode of two serial busses	x	-

H0012 CAN/LIN Bus Analysis

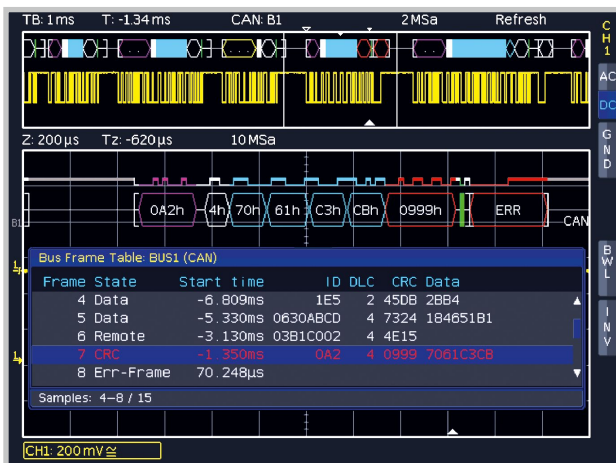
for all Oscilloscopes of the HMO Series



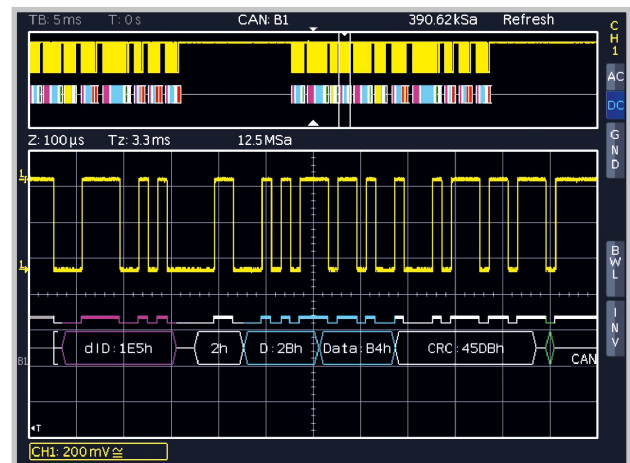
Mixed Signal and Bus Display



CAN Bus Configuration



CAN Bus list display



CAN Bus HEX

- ✓ CAN, LIN Bus Trigger and Decode
- ✓ Hardware accelerated Decode in Real Time
- ✓ Color Coded Display of the Content for intuitive Analysis and easy Overview
- ✓ More Details of the decoded Values come visible with increasing Zoom Factor
- ✓ Bus and List Display with synchronous Display of the Data
- ✓ Decode into ASCII, Binary, Hexadecimal or Decimal Format
- ✓ Up to four Lines to show the decoded Values
- ✓ Powerful Trigger to isolate specific Messages
- ✓ Option for all Oscilloscopes of the HMO Series, retrofittable

H0012

H0012 CAN/LIN Bus Analysis

CAN Bus		LIN Bus
Bus Configuration		
Bit rates	Pre-Defined or User-Select, 100 Bit/s...4 Mb/s (HM0352x/2524), 100 Bit/s...2 Mb/s (HM072x...202x)	Pre-Defined or User-Select, 100 Bit/s...4 Mb/s (HMO352x/2524), 100 Bit/s...2 Mb/s (HMO72x...202x)
Signal Type	CAN-L or CAN-H, Single Ended or Differential Probe (Analog Channels only)	n/a
Sample Point Range	25...90%	n/a
Threshold	Pre-Defined or User-Select	Pre-Defined or User-Select
Polarity	n/a	High or Low Active
Protocol Version	n/a	1.x, 2.x, J2602, 1.x or 2.x
Trigger		
Source	digital Channel LCH 0...15 [Opt. H03508], analog Channel CH 1...2 [CH 1...4]	digital Channel LCH 0...15 [Opt. H03508], analog Channel CH 1...2 [CH 1...4]
Event	Start of Frame (SOF), End of Frame (EOF) Error Frame Error condition: Stuff Bit Error, CRC Error, Not Acknowledge, Form Error Overload Frame Data Frame (11 or 29 Bit ID) Remote Frame (11 or 29 Bit ID) Identifier: 0, 1, X (Don't Care) Pattern, Trigger when =, ≠, <, > Identifier and Data: ID and 64 Bit data pattern (0, 1, X), trigger when =, ≠, <, >	Start of Frame (SOF), Wake Up Frame Error Frame Error condition: Checksum Error, Parity Error Synchronisation Error Identifier: 0, 1, X (Don't Care) Pattern, Trigger when =, ≠, <, > Identifier and Data: ID and 64 Bit data pattern (0, 1, X), trigger when =, ≠, <, >
Input format	Hexadecimal or Binary	Hexadecimal or Binary
Hardware accelerated Decode		
Source	digital Channel LCH 0...15 [Opt. H03508], analog Channel CH 1...2 [CH 1...4]	digital Channel LCH 0...15 [Opt. H03508], analog Channel CH 1...2 [CH 1...4]
Display Bus	color coded for Start and End of Frame: White brackets Data ID: Magenta, Remote ID: Yellow DLC: White, Data: Cyan, CRC: White ACK: Green, Overload: White, Error: Red up to four lines for decoded values, synchronous display of the Bit lines	color coded for Start and End of Frame: White brackets Break: Magenta, Synchronisation: White Identifier: Yellow, Parity: Green, Data: Cyan Checksum: White, Error: Red, Wake Up: Magenta up to four lines for decoded values, synchronous display of the Bit lines
Table	Display of Bus 0 or 1 Frame Number State (Frame Type or Error Description) Start Time, Identifier, DLC, CRC, Data	Display of Bus 0 or 1 Frame Number State (Frame Type or Error Description) Start Time, Identifier, Length, Checksum, Data
Format	Identifier & other: hexadecimal Data: ASCII, binary, decimal, hexadecimal	Identifier & other: hexadecimal Data & Checksum: ASCII, binary, decimal, hexadecimal